Amendments to the Specification:

Please replace paragraph beginning on page 3, line 10 with the following amended paragraph:

The subject ~~dynamic prefetch technique for a continuous burst read operation~~ "Dynamic Prefetch In Continuous Burst Read Operation" may be better understood by, and its many features, advantages and capabilities made apparent to, those skilled in the art with reference to the Drawings that are briefly described immediately below and attached hereto, in the several Figures of which identical reference numerals (if any) refer to identical or similar elements, and wherein:

Please replace paragraph beginning on page 12, line 6 with the following amended paragraph:

Directing attention now to COMPARE 22 in FIG. 2, COMPARE 22 is seen there to provide an address input 221. Address input 221 accepts latched PFADDR data from an output 235 of MUX 23. In addition, COMPARE 22 accepts RECADDR data at an address input 222. Furthermore, COMPARE accepts at input 223 the PFVALID signal from ADDR 21, the PWRDN signal (see above) at input 224, the ADV signal at input 225, and the CLK signal at input 226. COMPARE [[12]] 22 provides PFHIT at an output node 228. PFHIT assumes a first value (e.g., a logic level ONE) when COMPARE 22 determines that the prefetched address at input 221 is identical to the received address at input 222. PFHIT assumes a second value (e.g., a logic level ZERO) when the prefetched address and the received address are not identical. Accordingly, appearance of the first value at output 227 is designated a "hit," and the appearance of the second value at output node 227 is designated a "miss". As may be seen in FIG. 2, the PFHIT output of COMPARE 22 is coupled to input 233 of MUX 23 and is also distributed to memory array 30 in a manner that selectively enables or disables the data output of the memory. That is, in any one of a number of approaches that will be discerned by skilled practitioners, the application of PFHIT to memory device 30 causes appropriate data to appear at the output of memory device 30, regardless of the occurrence of an unanticipated interruption in the continuous burst read operation.

Please replace paragraph beginning on page 13, line 7 with the following amended paragraph:

Understand that specific aspects of the design and operation of memory device 30 do not constitute an aspect, or limitation on the scope, of the subject invention. Similarly, operation of the subject invention extends to numerous memory technologies, now ~~know~~ known or hereafter developed. Nonetheless, allusion to the salient common features of prevailing memory designs is considered here to contribute to an appreciation of the operation of embodiments of the invention. Assume, then, that memory device 30 is instantiated in the form of a more or less familiar flash memory, although other memory technologies are similarly candidate beneficiaries of embodiments of the invention. Accordingly, memory 30 will comprise an array of memory cells arranged in rows and columns. Each site in the array is populated by a cell, the design of which may incorporate one or more metal oxide semiconductor (MOS) transistors, or other suitable data storage devices. The array of cells is accessed through, for example, an address buffer that is coupled through address latches and address counters to row and column decoders. Selected cells are coupled to sense amplifiers that detect the (logical) contents of respective cells. The sense amplifiers are, in turn, typically coupled through a multiplexer to input/output (I/O) buffers. Consequently, although the subject invention contemplates all modalities that effect selective disabling (or enabling) of the data output of memory 30 in response to the value assumed by PFHIT, for convenience it may be assumed that the data output of memory 30 may be disabled simply be disabling the output buffers. In some circumstances, more elaborate approaches may be warranted or required to prevent the propagation of corrupt data from the memory array 30.

Please replace paragraph beginning on page 15, line 12 with the following amended paragraph:

Note that in the embodiment of FIG. 2, the PFADDR input [[121]] 221 of COMPARE 22 is provided by output 235 of MUX 23. In the referenced embodiment, MUX 23 comprises address data latches, so that output 235, and of course, the PFADDR input 221 to COMPARE 12, are latched. In this manner, the PFADDR input to COMPARE 22 is preserved ~~in tact~~ intact, irrespective of anomalies that may arise in the course of burst read operation.

Please replace paragraph beginning on page 16, line 20 with the following amended paragraph:

Attention is here directed to FIG. 3, which constitutes a timing diagram that articulates the temporal relationships between significant signals introduced above, as these signals may arise in accordance with one embodiment of the invention. As may be seen in FIG. 3, the set of time-variant and interrelated signals defined therein include the RECADDR 31, system clock (CLK) 32, ADV 33, PFADDR 34, PFDONE 35, PWRDN 36, PFHIT 37, ADDROUT 38 (at

ADDROUT output [[136]] 236 of MUX 23 in FIG. 2), and DATA OUT 39. Initially, at time 311 a received address, REC0 appears from, for example, a system processor. Reception of the address REC0 is coincident with the rising edge of CLK 32 that appears at time 321, as well as with the falling edge of ADV that occurs at time 331. Because the address received at the time 311 is, for purposes relevant here, assumed to be the initial received address, output 136 of MUX 13, ADDROUT, will assume a value of ADRO0 at time 381, also coincident with times 311, 321 and 331. Assuming, for pedagogical purposes, that the memory read latency is six CLK periods, then corresponding data will appear at the memory output at time 391, six CLK cycles after the reception of the initial received address at time 311. At time 341, the RSM prefetch address generator outputs the first prefetched address PF1, resulting in a PFDONE pulse that has a rising edge at time 351. Similar rising edges occur at times 352 and 353. The next corresponding received address, REC1, appears at time 312, after which the falling edge of ADV occurs at the time 322. Note that similar falling edges occur at times 333 and 334. Because, according to FIG. 3, the received address represents at hit, PFHIT assumes a logic level ONE at time 371. Consequently, output [[136]] 236 of MUX 13 selects the prefetched address, and PFADDR is coupled to the memory device. Corresponding DATAOUT appears at time 392. The next address cycle similarly results in a hit, and at time 384 the prefetched address, PF2, that is available at time 342 appears as ADDROUT. Corresponding data arrives at time 393. PFHIT persists at a logic level ONE. Note the various values of ADDROUT at times 382, 383, and 385.

Please replace paragraph beginning on page 18, line 3 with the following amended paragraph:

At time 343, 353, the sequential prefetched address PF3 is generated. However, at time 314 a received address REC3 appears that is not identical to the prefetched address at time 353. Consequently, at time 372, PFHIT reverts to a logic level ZERO. Additionally, at this time the output of MUX [[13]] 23 is selected to be RECADDR, and the appearance of the ADRO3 is simultaneously truncated at time 386. Note that ADRO3 is an address that corresponds to PF3, the disqualified prefetched address. ADRO3 is replaced by ADRO4, an address that corresponds to the received address REC3.

Please replace paragraph beginning on page 18, line 22 with the following amended paragraph:

The processor 410 may be coupled over a host bus 415 to a memory hub (i.e., a memory controller) 430 in one embodiment, which may be coupled to a system memory [[320]] 420 via a memory bus 425. The memory hub 430 may also be coupled over an Advanced Graphics Port (AGP) bus 433 to a video controller 435, which may be coupled to a display 437. The AGP bus 433 may conform to the Accelerated Graphics Port Interface Specification, Revision 2.0, published May 4, 1998, by Intel Corporation, Santa Clara, California.

Please replace paragraph beginning on page 19, line 18 with the following amended paragraph:

The memory hub 430 may also be coupled (via a hub link 438) to an input/output (I/O) hub 440 that is coupled to a input/output (I/O) expansion bus 442 and a Peripheral Component Interconnect (PCI) bus 444, as defined by the PCI Local Bus Specification, Production Version, Revision 2.1 dated in June 1995, or alternately a bus such as the PCI Express bus, or another third generation I/O interconnect bus. The I/O expansion bus [[342]] 442 may be coupled to an I/O controller 446 that controls access to one or more I/O devices. As shown in FIG. 4, these devices may include in one embodiment storage devices, such as a floppy disk drive 450 and input devices, such as keyboard 452 and mouse 454. The I/O hub 440 may also be coupled to, for example, a hard disk drive 456 as shown in FIG. 4. It is to be understood that other storage media may also be included in the system. In an alternate embodiment, the I/O controller 446 may be integrated into the I/O hub 440, as may other control functions.